

ULTRAFAST ANALOG-TO-DIGITAL CONVERTER USING RESONANT-TUNNELING TERNARY QUANTIZERS

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ABSTRACT

We study an analog-to-digital converter (ADC) that uses ternary quantizers consisting of resonant-tunneling diodes and HEMTs. This paper explains the ADC design and presents experimental results. A resonant-tunneling ternary quantizer operates at 10 GHz and a 2-bit ADC operates at 5 GHz.

1. INTRODUCTION

The application of resonant-tunneling diodes (RTD) to ultrafast circuits has been extensively investigated recently [1, 2, 3] because of the ultrafast switching speeds of RTDs [4] as well as their functionality, which leads to reduced circuit complexity. One possible application of these devices is an ultrafast analog-to-digital converter (ADC) [3, 5], which are attractive for wireless communications because they help realize the full potential of digital receivers. In addition, when resonant-tunneling diodes are connected in series, negative differential resistance results in multiple-peak I-V characteristics, which are well-suited for implementing multiple-valued logic (MVL) circuits [6]. MVL is expected to help make the circuit configuration simpler compared with conventional binary circuits. A compact ADC using quaternary quantizers has recently been presented with possible multi-GHz operation [7].

In this paper, we propose another approach to the

construction of ultrafast ADC, in which ternary quantizers are used instead of quaternary ones. By using ternary quantizers, we can enhance the operation margin and reduce the circuit voltage, while still maintaining the advantage of the MVL. This has led to the first experimental demonstration of an ultrafast operation of ADC with MVL circuits, which is described in this paper. We first explain the operation principle and then present experimental results for a 10-GHz HEMT-driven ternary quantizer and a 5-GHz 2-bit ADC.

2. PRINCIPLE OF ADC OPERATION WITH TERNARY QUANTIZERS

The ADC consists of ternary quantizers (TERNs), which quantize the input analog signal into three-level output. The TERNs are followed by encoding circuits (ENCs) that convert the ternary input to binary output. Figure 1(a) illustrates a block diagram of a 3-bit ADC, as an example. Figure 1(b) shows its operating principle and the functions of the TERNs and ENCs. TERN quantizes the input into three-level output, “0”, “1”, and “2”, with two threshold voltages. ENC then converts the three signals to “low”, “high”, and “low”, respectively. Using this low-high-low output as an element of the Gray code and suitably designing the threshold voltages, we can obtain a 3-bit Gray-code output, as depicted in Fig. 1(c). ADCs with 4-bit or

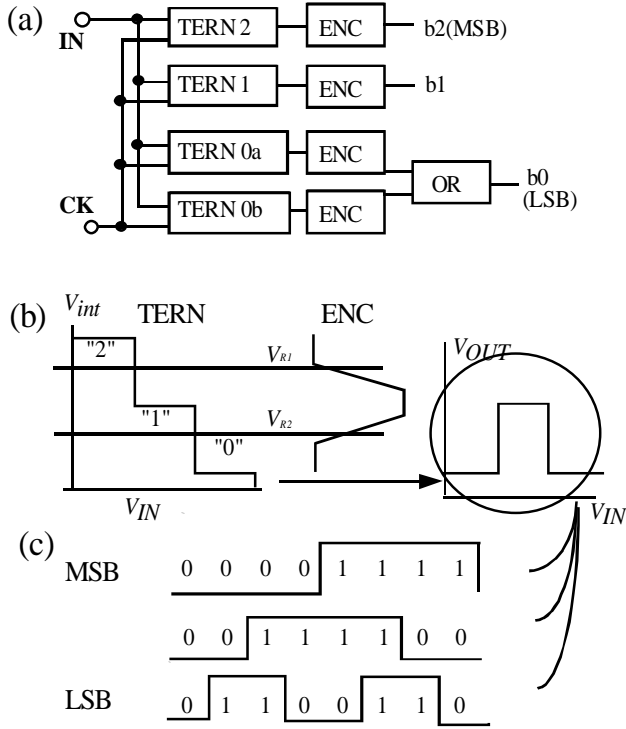


Fig. 1: (a) Block diagram, (b) schematic explanation, and (c) output binary code of a 3-bit ADC using ternary quantizers.

higher resolutions can be achieved in a similar manner.

The ternary quantizer (TERN) is a monostable-to-multistable transition logic (MML) circuit [6] consisting of four RTDs (A, B, X, Y) and two HEMTs, Q1 and Q2 [Fig. 2 (a)]. Q1 is used to effectively modulate peak currents of RTDs X and Y while Q2 is used to supply a clock signal for the quantizer. An encoding circuit (ENC) contains eight HEMTs, and is comprised of a source-follower and a folding circuit based on differential amplifiers, as shown in Fig. 2(b). The output voltage of an ENC is “high” only for the input voltage between the two reference voltages V_{R1} and V_{R2} ($V_{R1} < V_{R2}$), otherwise it is “low”.

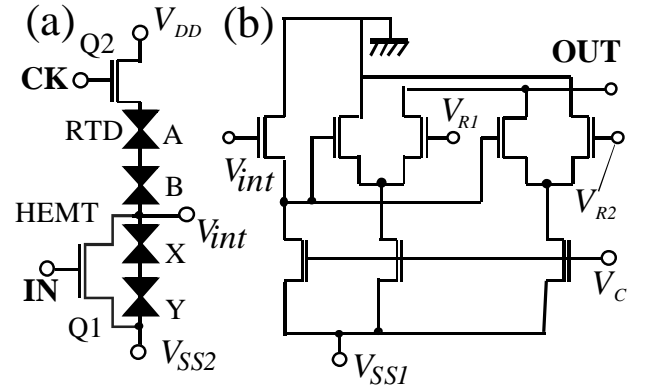


Fig. 2: (a) Ternary quantizer TERN and (b) encoding circuit ENC.

3. EXPERIMENTS

3.1 Fabrication

We integrated InGaAs/AlAs/InAs RTDs and InAlAs/InGaAs HEMTs on a semi-insulating InP substrate[8]. The cross-sectional view of a fabricated device is shown in Fig. 3 (a). The RTDs had a peak voltage of 0.3 V and a peak-to-valley current ratio of 10. Peak current density was 9.5×10^4 A/cm² and the standard deviation of peak currents for a 4- μm^2 RTD was as low as 3% over a 2-inch wafer. An InP recess etch-stop layer was inserted in a HEMT barrier layer. We used a MBE regrowth technique for RTD layers, which were grown on the MOCVD HEMT layers [9]. The gate length of the HEMT used was 0.7 μm , the average threshold voltage was -0.50 V, and the standard deviation was 47 mV. The f_T of HEMT fabricated by a similar process was 40 GHz.

3.2 2-bit ADC design

A block diagram and micrograph of the fabricated 2-bit ADC are shown in Figs. 3(b) and (c). In this ADC, we used RTD areas ranging from 4 to 9 μm^2

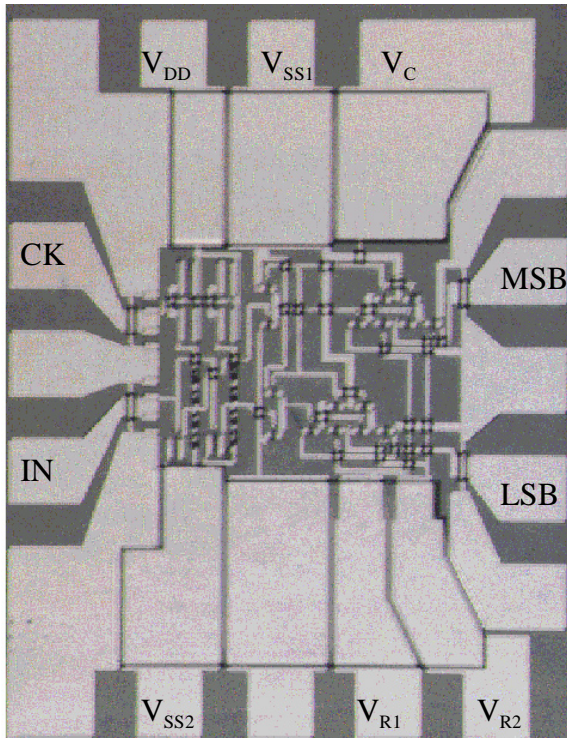
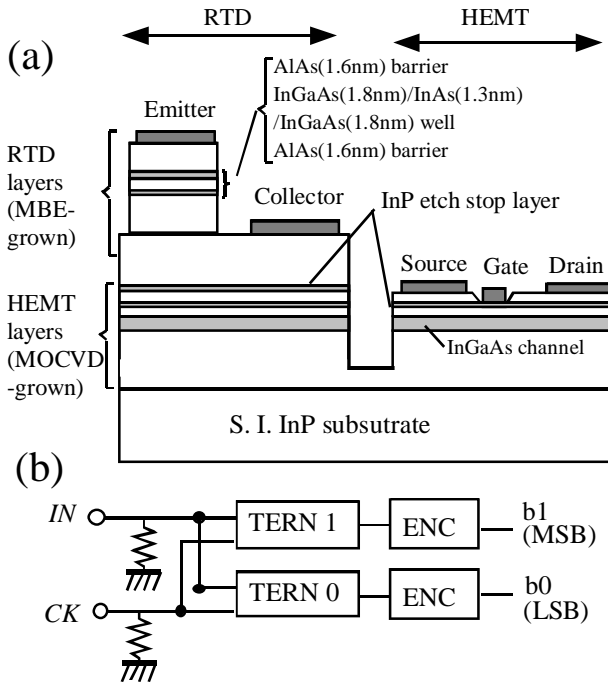


Fig. 3: (a) Cross-sectional view of fabricated devices, (b) block diagram of a 2-bit ADC, and (c) chip micrograph (1.0 x 0.8 mm²).

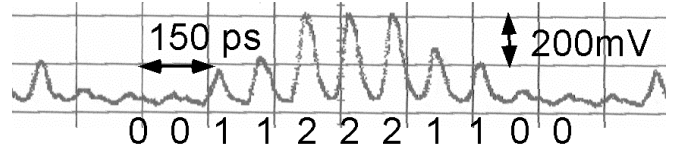


Fig. 4: Output waveform of a ternary quantizer. (10 GHz)

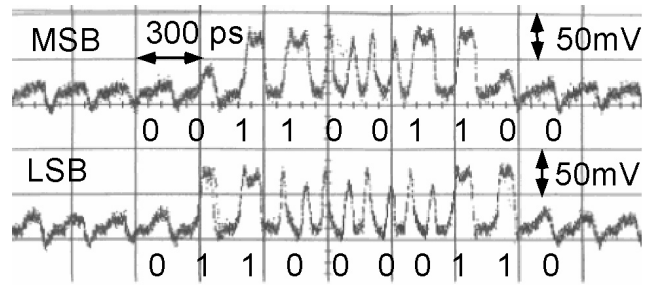


Fig. 5: Output waveforms of a 2-bit ADC (5 GHz).

to obtain the desired threshold voltages. The whole 2-bit ADC contained 8 RTDs and 20 HEMTs. The voltage sources were $V_{DD} = 0$ V, $V_{SS1} = V_{SS2} = -3.2$ V, $V_C = -0.1$ V, $V_{R1} = -2.3$ V, and $V_{R2} = -1.4$ V.

3.3 Measurement results

The devices were measured at room temperature on a wafer prober. Sinusoidal clock and input signals were supplied by synthesized signal generators. The output waveform of the ternary quantizer is shown in Fig. 4. A three-valued output waveform is observed at a clock signal of 10 GHz and an input signal of 1 GHz. Figure 5 plots the measured output waveforms for the 2-bit analog-to-digital converter for a clock signal of 5 GHz and input signal of 400 MHz with an amplitude of 0.5 V and centered at -3 V. Return-to-zero type 2-bit Gray code output was successfully confirmed. The lower operation frequency (5 GHz) of the ADC compared with that of the quantizer (10 GHz) is probably caused

by the encoder circuits. There is still much room to improve the encoder circuit configuration for better performance.

4. CONCLUSION

We described an analog-to-digital converter that uses ternary quantizers consisting of RTDs and HEMTs. The experimental results were presented, and the ternary quantizer was shown to operate at 10 GHz, while the 2-bit ADC operated at 5 GHz.

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